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In the claims: The claims are as follows.

- 1. (Original) A semiconductor component (30) having a siliconbearing layer (32) and a praseodymium oxide layer (40), characterized in that arranged between the silicon-bearing layer (32) and the praseodymium oxide layer (40) is a mixed oxide layer (34) containing silicon, praseodymium and oxygen, which is of a layer thickness of less than 5 nanometers.
- 2. (Original) A semiconductor component as set forth in claim 1 wherein the mixed oxide layer (34) is of a layer thickness of a maximum of 3 nanometers.
- 3. (Previously presented) A semiconductor component as set forth in claim 1 wherein the mixed oxide (34) is a pseudo-binary, non-stoichiometric silicate or an alloy of the type  $(Pr_2O_3)_x(SiO_2)_{1-x}$ .
- 4. (Currently amended) A semiconductor component as set forth in claim 3, wherein the mixed oxide (34) is an alloy of the type  $(Pr_2O_3)_x(SiO_2)_{2-x}$ , and wherein x increases from a first value at an interface of the mixed oxide layer with the silicon-bearing layer (32) to a second value at an interface of the mixed oxide layer with the praseodymium oxide layer (40).

The mixed exide layer is a  $(Pr_2O_4)_{+,*}(SiO_4)_{+,*}$  layer wherein the coefficient  $\kappa$  at the interface 36 is of a value 0.3 and at an interface 38 to an adjacent praceodymaum exide layer  $(Pr_*O_4)$  40 it is of a value 1.

- (Previously presented) A semiconductor component as set forth in claim 1 wherein the silicon-bearing layer (32) comprises doped or undoped silicon-germanium.
- 6. (Previously presented) A semiconductor component as set forth in

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claim 1 wherein the silicon-bearing layer comprises doped or undoped silicon.

- 7. (Previously presented) A semiconductor component 30 as set forth in claim 5 wherein the silicon-germanium layer or the silicon layer has an (001) orientation at the interface to the mixed oxide layer.
- 8. (Previously presented) An MOSFET as set forth in claim 1.
- 9. (Previously presented) A memory cell as set forth in claim 1.
- 10-21. Withdrawn.